Patent Application of

Ted Humphrey

for

TITLE: Symmetrical Current Amplifier

CROSS-REFERENCE TO RELATED APPLICATIONS

There is co-pending patent application to this one. The Title is Analog Electronic Device and the Applicant is Ted Humphrey. It also is being filed in July 2003. It claims, in one of its dependant claims, the use of the teaching of that proposed device to create an amplifier where the amplifier could under certain conditions be viewed as a current amplifier, which is the subject of this patent application. The current amplifiers as detailed in the co-pending patent application depend on the teaching of that patent for their existence. Therefore the amplifiers taught in that patent could not be included in this patent. Those teachings show new unique ways to design an amplifier using a basic device, the core of that patent, that are an improvement over what could be designed before that invention. There is no common structure taught in the two patents.

Description

TECHNICAL FIELD

This invention relates to the creation and use of electronic current amplifiers. The invention teaches a topology, really a family of topologies, that can be used to create amplifiers with 2 inputs that are responsive to input current. It further teaches how to extend this topology and the use of current amplifiers to get improved performance and simplicity.

Prior Art

After the advent of transistors, the transition to differential amplifier circuits was swift. Traditionally, most amplifiers have been based on a "long tailed pair". The advantages affected most spheres of use.

Examples are to be found in early reference works such as the *Transistor Manual* from General Electric of 1964. Starting on page 111 is a complete analysis of the differential amplifier circuit.

Early U.S. patents such as 3,541,465 titled *Transistor Differential Amplifier Circuit* by Nagata (1970) show advancements to the basic circuit; in this case cascoding the input transistors. Whereas Patent RE30,587 by RCA (1981) was an improvement in the buffering of the output, where with feedback, the output voltage can be forced to

some useful level. The circuit depends highly upon matching of transistor V_{be} voltages for it DC stability and operation.

The basic endeavor of an amplifier (circuit) is to "examine" the input(s) and produce an output that is a multiple of the difference of the inputs. The input difference is usually a voltage and the output is a voltage. It is usually desired that the output is referenced to some useful reference point, generally ground. This aids in applying negative feedback to the circuit. If the DC deviations between the input and the output of the amplifier are too great then biasing and feedback become too complicated. Other DC concerns are offset, bias current, and drift. There can be AC deviations also. AC concerns include: frequency response, clipping, and distortion products such as harmonic distortion, inharmonic distortion, power supply induced distortion and slew rate limiting (internal saturating of transistors).

The use of the long-tailed pair works by converting a voltage difference to a current difference. Most early non-differential circuits converted a voltage input to a current across a resistor thus producing a voltage. In Figure 1, voltages V_{in1} and V_{in2} produce currents that flow through R_{L1} and R_{L2} producing voltages V_{out1} and V_{out2}. The bipolar transistor is ill suited to converting a voltage to a current much less a voltage to a voltage, which it can not do directly. Much of the research in design of transistor circuits has been in the direction of handling the problems associated with this converting of a voltage difference to a voltage. Some DACs use currents to develop speed and accuracy and some digital circuits use current steering for speed. Otherwise, in a voltage domain, handling items such as Miller Effect, hard saturation, Early effect, biasing instabilities, level shifters, phase inverters, buffering, etc. becomes the problem.

One might try to consider the use of a transistor in a common-emitter configuration as a current amplifier BUT I am not aware of any prior art showing such a usage. The reasons are obvious. The problems are too many and too great to ever create a useful circuit. The problems include offset – the output voltage not being close enough to the input voltage to allow negative feedback , biasing stability, common mode limits, no good way to use feedback to control the gain without affecting biasing, etc.

With time, we see the advent of Current Feedback Amplifiers (CFAs). This advancement helps the art of electronics as it forces the amplifier to work more in the current domain. Patents 4,502,020 and 4,713,628 by David A. Nelson of Comlinear (1985 & 1987) are basic. Improvements are included in patent 5,786,731 by National Semiconductor. We have also the Diamond Circuit of Burr Brown. The cleanest example (schematic) is the simplified circuit of the LM6181 by National (or elantec EL2020 or Burr Brown OPA603) and reproduced as Figure 2. This circuit is typical as Current Feedback Amplifiers are usually built around the same circuit for the input and output. That circuit is called by various names including a LH0002 (or just "0002") circuit or more recently a "4-transistor emitter follower" in Patent 6,166,603 by Douglas L. Smith in his Figure 1 and in the text of his patent. Transistors Q_{301} , Q_{302} , Q_{303} , and Q_{304} form the input buffer and Q_{312} , Q_{313} , Q_{315} , and Q_{316} form the output buffer in Figure 2.

These CFA circuits generally have the following faults/weaknesses:

a) depend on emitter followers (for both input and output)

b) don't really have an inverting input but cheat and use an "output" as a low impedance input

c) with a low impedance "loading" the inv_input, as is intended under normal operation, the input stage of the circuit become a unity gain voltage buffer that has inherent non-linearity's (distortion) due to shifting DC levels, Miller Effect, Early Effect, etc. It is acknowledged in the industry that CFAs are not low distortion!

d) depend on the match of V_{be} voltages for the biasing of the circuit

e) buffer the output with complicated emitter circuits which still depend on matching transistor V_{be} voltages. See patent 5,786,731 by National Semi. (1998). See also National LM6181.

National has attempted to handle the problem of the low-impedance input by buffering that input with another input stage in their LM6171. This is an obvious solution that had been around and is best expressed by Burr Brown in some of their materials. In Burr Brown Application Bulletin AB-183, they detail what they call the DIAMOND CIRCUIT that is used in the OPA660 and OPA622. Nevertheless, the circuit still does not handle the basic weaknesses of the topology/structure/architecture.

There are a family of patents that pertain to input stages that have some structure similarity.

4,357,578, 6,486,737 and 4,918,398 are not current amplifiers. 4,357,578 by Yokoyama 11/2/82 includes a system of resistors connecting the emitters of the input transistors. The drawings all includes either notations of voltage inputs or include resistors to ground at the inputs. Internally any signals are converted to voltages. The Yokoyama circuit is not as simple as proposed in this application and there is no teaching of anything close to that of a current amplifier. 6,486,737 has gm normalizing circuits that preclude the use of current inputs. 4,918,398 uses level shifters and input resistors for biasing in an interaction that also would preclude the use of current inputs.

The following are neither symmetrical not current amplifiers: 4,555,673, 4,532,479, 5,714,906, 4,977,378, 5,294,892, 5,294,893, 5,153,529, 5,140,280, and 6,518,842.

Two of these owned by Signetics Corporation are representative. 4,532,479 Blauschild 7/30/1985 and 4,555,673 Huijsing et al. 11/26/1985. In the Blauschild patent, all drawings show a non-symmetrical amplifier. The patent repeatedly refers to "output signal at terminal 21 follows the voltage difference between terminals 1 and 2" or "amplifying a voltage difference between terminal 1 and 2". The "description of the preferred embodiment" explains in detail how changes in voltage input create changes in the output. Even computes voltage amplification at 50 to 300 and 30 to 120. Explains how "some or all of the bipolar transistors may be replaced with FETs." It is clear that the use of the patent is for voltage amplification. There is nothing in the patent that teaches anything about current amplifiers. The claims don't claim anything and the teaching in the rest of the patent don't teach anything that would lead someone to build a symmetrical current amplifier. In 4,555,673, the area of concern is common mode range and constant gm over input voltage range. The inputs of all the amplifier drawings show the inputs as voltages. Included is additional circuitry to change the function of the amplifier depending on the input common mode voltage. The embodiments in that patent won't work with current inputs. Document 98-2000-450

BA/RP2.5MFP0785 from Signetics in 1985 adds details of the implementation of the patent in describing the SA/SE/NE5230. It reinforces that the design is non-symmetrical and is intended to respond to voltage inputs. In fact it defeats 1/2 of the input structure at a time, making it impossible to function as a current amplifier. The structure of the circuitry in the patent is very different from that proposed in this patent application. That patent teaches a voltage input amplifier with improved handling of common mode input voltage and gm over voltage. This application teaches "symmetrical current amplifiers" with simpler topologies. So the structure, function and results are different.

This whole family of patents are directed toward handling gm normalization and extending common mode range. Both of these concerns deal ONLY with an amplifier when used in a non-inverting configuration. That is what these patents are about. In fact, when used in an inverting configuration, they generally revert back to a long-tailed pair differential voltage input amplifier.

In Patent 5,396,194 Williamson, Audio frequency power amplifiers, there is shown in Figure 24C, a subsection showing some structure that is similar to that proposed in this patent. In that drawing, even though it appears similar, it is a voltage amplifier. It compares a voltage input to the output voltage and produces voltages both internally and externally. This is evident by the fact that the output is connected to an inverting input directly without a resistor. Thus, even though there appears to be some possible structural similarity, the actual structure, the function, purpose and results are different. There is no way that the subsection as detailed in the drawing could be used or converted to a current amplifier. It does not show to anyone viewing it the need for, or how to construct a true current amplifier. There is nothing in the drawing or patent that teaches what this patent does.

Summary of Invention

The object of this patent is to increase the art of electronics. This patent thus teaches the creation and use of current amplifiers. These are amplifiers that respond to current inputs rather than voltages, as is dominant in the field. It suggests the use of a family of topologies that function as needed in that the inputs do respond to currents. These topologies also have the low offsets that are needed to be able to use negative feedback. I have included equations that detail how to use the circuits that are built around these topologies. This is an advancement because with the ability to use amplifiers that respond to current feedback in a useful manner, we can design simpler circuits while getting higher performance. The key over prior current feedback amplifiers is that the prior amplifiers actually only have one current input and that input is really the output of a buffer and therefore is very current hungry. That forces the amplifiers to be operated as non-inverting amplifiers in the main to get frequency response and reduce offset. That is not the case with this patent as the amplifiers that result have two current inputs that are well behaved. Thus they can be operated in the inverting configuration. A preferred mode as it leads to lower distortion. The embodiments detailed center around the use of dual amplified (buffered) current subtractions at a high impedance point.

Symbols and Equations

The capital letter Q with a subscript represents transistors. Transistors with the same subscript perform a similar function in the different drawings (amplifiers). The circuits build from simple to more complex.

A capital letter I with a subscript indicates a constant current source in the drawings. If the subscripts are the same, then the value of currents are the same. This value of current can be altered to change the performance of the circuit. It can be optimized for the desired usage of the amplifier and the properties desired. Discussion of this is included in the DISCLOSURE OF INVENTION.

The capital letters A, B, C, D, E, F, G and V are used to indicate connection to the world outside of the amplifier itself. The letters A and B represent the inputs. C and D are outputs and are labeled such that a negative current "into" A or B will create a positive current from C or D respectfully and are therefore inverting inputs. E and F are internal summing points of the amplifier and with this connection the current gain can be controlled from outside the amplifier to configure the amplifier in some manner. G is also an output and is related by phase as detailed in the body of text. V with a subscript and a polarity indicate a connection to a supply voltage of some useful value. I_{in}, V_{in}, I_{out}, and V_{out} are exactly what is expected, they label the input current/voltage and the output current/voltage.

Use of capital letters R and Z are used to represent an impedance, either simple or complex. The use of R is a special case of Z as it represents a simple resistance. Generally the two are used interchangeably in this patent. Generally, any time a resistor is shown exterior to the amplifier, it could be a complex impedance rather than a simple resistance. For clarity, this document will try to state when it is important or when observations can be make about the nature of that impedance as it relates to the functioning of the amplifier.

In the same manner, the use of the word "source" is intended to include "sink" depending on the polarity of the transistors involved. Also, the words "accepts" and "produces" do not imply a direction of flow (current) or a polarity of voltage.

β always indicates the beta of a bipolar transistor and does not relate to feedback factors. It is generally in the range of 20 to 200. I generally estimate it at 100 for convenience.

Any equations included in this document are derived intuitively and are to show general properties of the circuit. They are first order approximations and are not meant to be necessarily a complete representation of the circuit. They are nevertheless offered as useful in understanding the workings of the circuit. There is much that is new here and so much work is yet to be done on an "academic" level fully detailing the properties of the circuits. This I leave to others as the included equations are sufficient to build workable/useful amplifiers.

Description of Drawings

Figure 1 shows prior art for a voltage differential amplifier.

Figure 2 shows prior art example of a Current Feedback Amplifier. This schematic is representative of many commercial integrated circuit amplifiers including National LM6181, élantec EL2030C, Burr Brown OPA623, Texas Instruments THS3001 and Comlinear CLC401.

Figure 3 is a dream circuit that is non-functional. Used as a point of departure.

Figure 4a shows the most simple embodiment of the teachings of this patent. It is a fully functional differential current amplifier. It relates to Claims 1, 2, 4, and 6.

Figure 4b shows a usage of 4a with one output connected to ground. It relates to Claims 1, 3, 5, and 14.

Figure 5 shows the amplifier of Figure 4a with one of the outputs disabled so that there are two inputs and only one output. The amplifier is a differential current amplifier where the difference of input currents produces a current output. The figure relates to Claims 3, 5, and 16.

Figure 6 shows a modification of the circuit, where with the addition of another stage following one half of the amplifier, that produces a circuit where both the outputs are in phase. This circuit is useful when hooked up properly. See also figure 13. This figure relates to Claims 11 and 12.

Figure 7 shows a modification of Figure 4 or 6 with only one output but still two differential inputs. This figure relates to Claims 3, 5, 14, and 17.

Figure 8 shows an improvement on the basic circuit to handle some of the restrictions on usage. It relates to Claims 1, 2, 4, 7 and 24.

Figure 9 shows an embodiment of the patent with the output of one side disabled and the other side buffered. It includes an internal summing point to allow control of the gain and frequency response of the amplifier. Note that there are still two current inputs but with the use of an impedance connected to point F, the output now should be considered a voltage. If the point F is not loaded with an impedance so as to create a voltage at the summing point, then the output should still be considered a current. This figure relates to Claims 3, 5, 14, 15, 18, and 19.

Figure 10 shows an embodiment with both sides of the amplifier buffered. It has consequently two summing points, noted as E and F. This figure relates to Claims 1, 2, 4, 8, and 10.

Figure 11 shows a modification of figure 8 where the quiescent current of all the transistors, $Q_1 - Q_8$, $Q_{21} - Q_{24}$, are substantially the same. This embodiment gives improved high frequency response. This figure relates to Claims 1, 2, 4, and 20.

Figure 12 shows a modification to the circuit in figure 10 where the all the transistors have substantially the same quiescent current. Even with this number of transistors the biasing is simple, uniform and stable. This figure relates to Claims 1, 2, 4 and 8.

Figure 13 shows the circuit of figure 6 with additional components that allows the ganging of the two halves of the circuit to produce an amplifier that has only one current input and one current output. Output C is out of phase with the input A and so negative feedback can be applied to the circuit. This figure relates to Claims 11 and 13.

Figures 14 and 15 show block diagrams of the amplifier circuit.

Figures 16 and 17 are used to determine the single ended open loop gain and closed loop gain of the amplifier.

Figures 18, 19 and 20 are used to determine the closed loop gain of the amplifier.

Figures 21, 22, 23, and 24 along with 18, 19 and 20 are used to examine the offset of the amplifier.

Disclosure of Invention

While examining the subject of amplifying circuits and the weaknesses of different architectures, I made two advancements. This patent is the subject of one of those.

Using as a stable datum that bipolar transistors work best in a current mode, I worked out a new approach to amplifying.

I kept coming back to the circuit of Figure 3. I just couldn't figure out how to get it to work. Finally I came up with the solution as detailed in this patent.

I knew I had to work with current. I knew that I had to handle items such as Miller Effect, hard saturation, Early effect, biasing instabilities, problems with level shifters and phase inverters, buffers, and the points mentioned about as a-e.

Figures 4a and 4b are first steps. The circuit in Figure 4a is composed of transistors Q_1, Q_2, Q_3, and Q_4 along with two current sources I_{cc}. It accepts two current inputs and outputs a current between C and D equal to $\beta * (I_B - I_A)$ (or from C to Ground and from Ground to D). This circuit has some limitations concerning common mode range – both current and voltage. BUT it does do a lot and gives a great place to start. It is a fully workable circuit. It just works best under certain conditions.

Figure 4b is similar but has only one output. Any current that would have flowed from C in Figure 4a is shunted to ground. The current out from D is still equal to $\beta * (I_A - I_B)$. Connecting resistors to the amplifier, either Figure 4 or 4b, as shown in Figure 16, we can work out equations for the amplifier. With A grounded (generally through a

resistor), then $I_D = -\beta * I_B$. Looking to Figure 16, with an input resistor R_{in}, A connected to ground and output resistor R_L (to ground), then $V_{out} = I_{out} * R_L = -\beta * I_{in} * R_L = -\beta * V_{in} / R_{in} * R_L$, then $A_{ol} = V_{out} / V_{in} = -\beta * R_L / R_{in}$. We now have the open loop voltage gain of the circuit. This is a similar equation to that associated with CFAs. Using feedback resistor of R_f as shown in Figure 17, and calculating the Loop Gain, we get Loop Gain = $(-\beta * R_L / R_{in}) / (-R_f / R_{in}) = \beta * R_L / R_f$. Again a similar equation to that of a CFA where the loop gain is a function of the feedback resistor but independent of the closed loop gain of the circuit. In usual terms of CFAs, the transresistance is simply $\beta * R_L$.

Figure 5 handles some of the common mode problems. In particular if one locks (connects) A to ground, then $I_D = -\beta * I_B$ with some limits to common mode voltage range. Alternatively, one can lock (connect) B to ground and $I_C = +\beta * I_A$ again with some common mode voltage limits.

Figure 6 is an interesting circuit. Its main usage is displayed in Figure 13. The circuit is derived from Figure 4A with the addition of transistors Q_5 and Q_6. Input A is an inverting input for both C and G. Input B is a non-inverting input for both C and G. Feedback can only be from one of the outputs to input A. The output at the other output would be affected by the input signal and by the loading on the other output with feedback attached and would be a current output independent of the load impedance at the "unregulated" output. Any voltage could end up much larger or smaller very easily. The outputs differ by a factor of beta even before this adjustment. Even if both loads were the same, one would get more current than the other load by a factor of beta. One could also ground one of the outputs. A resistor at output C would have affects on the input common mode range as any voltage imposed there would "appear" at input A.

Figure 7 is an improvement with regard to common mode limitations with just only one output. The voltage imposed on the inputs by any voltage generated at an output can be figured. Looking at Figure 16 – 22, we see that such a voltage is the same as the reference point for the load. In other words, if the amplifier has a load that is attached to ground and a feedback resistor, then the input point A will be at ground because practically zero offset current needs to flow through the feedback resistor. Or if B is attached to ground, then the input A will be forced the ground by the subtraction and addition of V_{be} voltages of the input transistors Q_1, Q_2, Q_3, and Q_4. In Figure 7 the circuit will function as long as this reference voltage is kept at least a certain distance from the rail voltages. Same equations as above hold true for this circuit with a transresistance of $\beta^2 * R_L$.

With Figure 8, we leave behind common mode voltage problems. Here we add transistors Q_7 and Q_8 to unload any output voltage that may be created by the output currents from reflecting back to the inputs, thus unlocking the input terminals. Inputs A and B are Inverting and Non-Inverting Inputs as respect to Output C (and visa versa with respect to Output D). See Figure 15, then $I_C = \beta^2 (I_B - I_A)$ and $I_D = \beta^2 (I_A - I_B)$. With A shorted to ground (generally through a resistor), then $I_D = -\beta^2 * I_B$. Looking to Figure 16, with an input resistor R_{in}, A connected to ground and output resistor R_L (to ground), then $A_{ol} = V_{out} / V_{in} = -\beta^2 * R_L / R_{in}$. This is a similar equation to that associated with CFAs. Using feedback resistor of R_f as shown in Figure 17, and calculating the Loop Gain, we get Loop Gain = $(-\beta^2 * R_L / R_{in}) / (-R_f / R_{in}) = \beta^2 * R_L / R_f$. Again a similar equation to that of a CFA where the loop gain is a function of the feedback resistor but independent of the closed loop gain of the circuit. In usual terms

of CFAs, the transresistance is simply $\beta^2 * R_L$. The best references regarding transresistance of CFAs is Burr Brown Application Bulletin #193 *THE CURRENT-FEEDBACK OP AMP A HIGH SPEED BUILDING BLOCK* by Anthony D. Wang, and *Analog Circuit Design* (Edited by Jim Williams) Chapter 25 *Current-Feedback Amplifiers* by Sergio Franco. Note that the transresistance of the CLC401 is $\approx$ 710KΩ with a break frequency of 350KHz which gives a product of 250 x 10^9. This is per data from Comlinear Corporation 1993-1994 Databook *Solutions with Speed* page 11-6 titled simply AN for Application Note. Normally this circuit from Figure 8 will be operated as shown in Figures 18 and 19. A true high performance fully differential amplifier. Because the load is not referenced to ground, the common mode voltages at A, B, C, and D will float to the most influential reference. We don't expect to see much D.C. voltage on the resistors in Figure 18 as current from the output (and possibly the input) will stabilize the circuit. Therefore if there is no reference connection between the input circuitry and the output circuitry, the amplifier will arrive at some compromise value. The current to determine that value will go though the resistors of Figure 18. If there is a common reference between the input and output, that value will be used as the common mode point of the points A, B, C, and D. This can be seen more clearly in Figure 19.

Figure 9 is a modification of 8 with one output buffered with a buffer similar to that used in prior art circuits i.e., LM6181. The buffer is created by transistors Q_9 through Q_{14}. A better buffer could be used here.

Figure 10 with both outputs of the circuit buffered. The second buffer is created by transistors Q_{15} through Q_{20}.

Of interest in Figure 10 is the biasing and gain. Each of the input transistors draws ½ I_{cc} current. This current is split by each of the next stage transistor's bases so that their collector currents is ¼ β I_{cc} as are all the other transistors. This means 6 stages drawing ¼ β I_{cc} for a total of 1.5 β I_{cc}. The amount drawn by the input transistors is over-shadowed and so the total $\approx$ 1.5 β I_{cc} for the whole circuit assuming that is β fairly uniform among the transistors.

Points E and F (Figure 10) are current summing/subtraction points as controlled by the input currents. These points can be loaded with a resistor, capacitor, combination or none. See figure 20. These establish the open loop gain of the circuit. Looking at each possibility separately.

a) **Resistor**. Assuming that R_E (and R_F) each to ground are smaller (by at least an order of magnitude) than the impedance at that point as determined by the "input impedance" of the following buffer section, which in this case is $\beta^2 * R_L$, then the open loop gain of the circuit is $-\beta^2 * R_E / R_{in}$. Loop gain then becomes $\beta^2 * R_E / R_f$. The open loop gain is now buffered from the load and independent of closed loop gain. Further, the loop gain now can be controlled by the choice of the feedback resistor R_f or the summing point loading resistor R_E. This again is very similar to CFAs, with the transresistance of this circuit equal to $\beta^2 * R_E$.

b) **Capacitor**. If we represent the impedance of the capacitor by Z_E (which is equal to $(2\ \pi\ f\ \ C)^{-1}$) then open loop gain is $-\beta^2 * Z_E / R_{in}$. The transresistance is $\beta^2 * Z_E$. Loop gain then becomes $\beta^2 * Z_E / R_f$. This gives one the ability to control the loop gain over frequency and thus tailor the stability and closed loop frequency response of the circuit. In particular, one can swamp the roll-off effects of β^2 or compensate for the roll-off because a roll-off of 12db/octave which is inherent to β^2, could create instability.

c) **C mbinati n**. This is a more general case of b where Z_E is just a more complicated value depending on the impedance of a capacitor in parallel with a resistor. This allows even more ability to control the loop gain of the circuit. Transresistance equal to $\beta^2 * Z_E$. With the addition of the buffer, the transresistance is no longer tied to the load, i.e. R_L. This gives us a great degree of control over the characteristics of the amplifier. It also means that if Z_E is much smaller than the input impedance of the buffer over frequency, the amplifier will be able to drive capacitive loads with no stability problems. This ability can be enhanced by the design of the "buffer".

d) **None**. In this case, the impedance of point E (or F) is that of the input impedance of the buffer which is approximately = $\beta^2 * R_L$. The open loop gain now becomes = — $\beta^4 * R_L / R_{in}$ with a transresistance of $\beta^4 * R_L$. This is a very high figure and won't generally be realized because of imperfections of transistors, stray capacitance, leakage, etc. and should not be relied upon. A much more stable and predictable circuit can be created by controlling the impedance at these points E & F.

In any case, we can see from the above that the frequency at which the loop gain drops to unity can be extended/controlled considerably. These factors will not be discussed in full detail in this patent as they are not necessary to what is being patented. The exact equations can be worked out by someone skilled in the art. The circuit, though new, is very simple and once understood by a new practitioner can be used right away. This is part of the circuit's strength.

The embodiment circuits have the further advantage that they can be used with very small supply voltages. Circuits 4, 5, 6, 7, 8, and 11 can be used with supply voltages very small indeed. The supply voltages must be greater than $\pm$ ($V_{be} + V_{sat}$) where V_{be} is the largest base emitter voltage of any of the input transistors and V_{sat} is the smallest voltage that can be sustained across the constant current sources that supply the current to the input transistors. Circuits 9, 10 and 12 must have more voltage as they must support an emitter follower output and so need enough voltage to be able to drive it. We see then that the supply voltages for circuits 4, 5, 6, 7, 8 and 11 could be as low as maybe $\pm$ .6 volts (probably even less when engineered properly). This is a **total** of **1.2** volts total for the circuit. This is less than the 1.8 volts that are normally required by most low voltage circuits today. Of course with such low voltages, one must look closely to common mode considerations. Using inverting configurations referenced to ground, there are no common mode problems.

Further, with circuits 5,7,8 and 11, the input transistors can not enter into saturation under normal operation. This will greatly lower distortion in audio or other applications requiring accurate AC performance.

Still further, the input transistors in figures 7, 8 and 11 are naturally cascoded. This, of course, improves high frequency performance and it is done without the extra voltage overhead normally needed.

An examination of AC distortion shows that an Inverting Configuration will always give the best results, i.e. low distortion, etc. This is because a NonInverting Configuration has common mode factors that alter the biasing/DC points of the circuit. This altering of internal voltages causes harmonic and non-harmonic distortion not to mention saturation, slew rate limiting, changes in device characteristics, etc. This current patent teaches circuits that are designed to best take advantage of this fact that inverting circuits are lower distortion. Even though the proposed

circuits can effectively operate in a Non-Inverting Configuration, they perform best in an Inverting Configuration. When operated in Inverting Configuration, the Input Transistors operate in a near perfect state as regards dissipation, voltage, and current with no or little Miller Effect or Early Effect. Existing CFA designs are very difficult to use in an inverting configuration, because with a suitable feedback resistor, the input impedance becomes very small. For this reason, the CFA is almost always used as a Non-Inverting Amplifier. This is not optimum, as noted above, because during the process of amplifying, a non-inverting circuit continually alters its internal DC bias/set points. This introduces distortion. Further, with existing designs, when used either as a Non-Inverting or Inverting Amplifier, one can not control the frequency response because one can not use capacitance across the feedback resistor, whereas, with the proposed design, one can use a feedback capacitor to tailor the frequency response of the amplifier. This is possible because one has more direct control of the loop gain. I have built many amplifiers with capacitance shunting the feedback resistor. It is very easily done.

In all of the embodiments, when used in an Inverting Configuration, only under extreme conditions do any of the transistors ever turn off completely. This further enhances performance.

IF used with supplies of sufficient voltage, anti saturation circuits can be added for the "output transistors" in circuits 6 - 13. Better output "buffer" circuits can also be used in circuits 9, 10, and 12.

Another advantage of the proposed topologies is improvements in DC performance. The proposed circuit has two balanced inputs. Any input offset is current offset. This current offset and the input bias current can be viewed together. In fact, they are the same. The only current needed by the inputs is offset current to force the output to zero, that is $I_5 = I_6$. We can examine the offset produced in open loop and with only a feedback resistor. Looking at figures 19 – 24 and applying these to the amplifier of figure 8 will give us these figures. In figure 21 or 22, we see that if we assume the current needed by the circuit is via B and that therefore there is no current through R_{f2} and the voltage at C is zero, the current through R_{f1} is $I_{input} = I_5 * [(\beta_2 \beta_6 - \beta_1 \beta_5) / \beta_1 \beta_2 \beta_5 \beta_6]$. If the match of $\beta_2 \beta_6$ to $\beta_1 \beta_5$ is better than 200% (2 to 1) then $I_{input} = I_5 / \beta_2 \beta_6$. If $\beta_2 \beta_6 = 20{,}000$, then $I_{input} = 2\ \text{ma} / 20{,}000 = 100\text{nA}$ for a simple circuit and normal values of transistor beta. With a feedback resistor of 10KΩ, then the voltage offset at the output will be less than 1 mV. If the match is 10% (1.1 to 1.0) then $I_{input} = I_5 / (10 * \beta_2 \beta_6)$. If $\beta_2 \beta_6 = 20{,}000$, then with this close match, $I_{input} = 2\ \text{ma} / 200{,}000 = 10\text{nA}$. With a feedback resistor of 10KΩ, then the voltage offset at the output will be less than 100 μV. Reflected back to the input, the figures are lower yet. Note that the stated input current for the OPA603 by Burr Brown for the inverting input is 25 μA. This is approximately 1000 times more current needed that the device detailed above. This in part is the reason we can use reasonable values of feedback resistance without offset problems.

In figures 23 and 24, we see that if we assume no current is input at B and A and that the voltage at D will be the current difference of the currents I_6 and I_5. Assuming fairly balanced current sources, we expect that the base currents of Q_6 and Q_5 are the same and equal to $\frac{1}{2} I_{cc}$. The output current then would be $\frac{1}{2} I_{cc} (\beta_6 - \beta_5)$ which could be faily large of the order of magnitude of 10 to 100 * I_{cc}. Obviously operating the circuit open loop isn't practical, the same as with any high gain amplifier.

Looking to figure 19, if we assume all of the input current is delivered via R_{in1} into B and that none is supplied by R_{f1} then per the above computing of input current of 10nA though R_{in1}, we get for an input resistor of 1,000, the voltage offset at the output will be less than 10 μV. An input resistor of 100 Ohms would give an effective input offset at the input of only 1 μV.

Even taking in account the voltage drop of any current through a feedback resistor, we are lead to believe that the voltage offset at the output produced by any current needed to zero the output current, would be the input offset current dropped across the impedance at the input.

These are satisfactory figures and independent of closed loop voltage gain. Any drift with temperature will be caused by variation of the βs of the transistors. This variation is not nearly as drastic as the variation of current due to changes of V_{be} experienced in prior art circuits. In fact, β will generally increase with temperature and so can be expected to decrease any input current needed to produce a zero output current. Also, the input stage, 4 transistors $Q_1 - Q_4$, dissipates constant total power = $2 * I_{cc} * V_{supply}$. In fact, each transistor can only vary in power dissipation from 0 to 2X in extreme. When positioned near to each other either in an Integrated Circuit or on a PCB, the DC Stability of the circuit can be very good. The quiescent current of the output stage(s) will increase as the β of the output transistors increase because of the constant drive current (equal to half the constant current from the constant current sources that supply the input stage). If the β of the input transistors increases, then the offset current will decrease. If DC performance is the most desired feature of a design, the input and output stages can be used at a lower quiescent current along with high β transistors and one can easily realize a very high performance DC amplifier.

Normally, low voltage supplies have forced many op amps to be designed with FETs of one kind or another. Low supply voltages have not been kind to DC (or AC) specs in op amps. If one is just dealing with low voltages and can stay within certain common mode ranges, the proposed circuits are quite fantastic for DC amplifying. The dissipation of the transistors (or the entire circuit) at low voltages is very small indeed. This further adds to a very stable DC performance. An example: assuming one can use the circuit of Figure 4, with a supply voltage of ± .7 volts and a quiescent current of .2 ma, we see that there is total dissipation of 140 μW and the ability to drive 2500Ω loads to ± .5 volts. At these levels, there will be very little heating of the transistors and therefore very little variation of β, so almost nil variation of input current and therefore stable DC performance. With real attention to all the details for an application, it is possible to go much lower to ± .5 volts and quiescent current of 1 μA for a total dissipation of 1 μW. Maybe even lower! Please note, the open loop input impedance is always basically = $\beta * R_L$, so the circuit doesn't load itself.

Applying the above to a specific example, let us look at the measuring of currents where there is a wide variation. Assume a current is sensed by a .1 mOhm resistor (shunt). The top range is say a 100 Amps for a voltage drop of 10 mV. The dissipation of the shunt is 1 Watt. The question is how low can we go in measuring current through the shunt before we are swamped by offset problems. We set up our amplifier in a differential configuration with a gain of 1000 and use an input resistors of 10 Ohms and feedback resistors of 10,000 Ohms. For 100 Amps dropping 10 mV across the shunt, the output of the amplifier would be 10 Volts. Using an amplifier design which includes a

buffer, the input offset current would be less than 1 nA. This would create a voltage of 10 nV at the output of the amplifier. With a gain of 1000, this reflects back to an effective input offset voltage of 10 pV at the source. The amount of current across the shut to equal that amount of offset would be 100 nAmps. The range is from near 100 nAmps to 100 Amps, a dynamic range of 9 decades or 10^9. The voltage output is probably still below the noise floor of many instruments.

Circuits 4, 8, and 11 are equally good when used with low supply voltages to produce great DC performance.

High supply voltages are not needed to get good DC or AC specs.

Normally, even with CFAs, one computes on the "input impedance". This is a measure of interest. The input impedance of the Inverting Input of a CFA is very low as basically it is an output of a voltage buffer. This makes it hard to use. The Non-Inverting Input of a CFA is said to be high. That is because it is basically a voltage input. Only the Inverting Input is a current input and thus functions as a "current feedback" point in a Current-Feedback Amplifier. BUT we can see that in a CFA, the Inverting Input draws lots of current really. On the order of 25 μA. Using large resistors for feedback resistors leads to problems with AC Stability and DC offset problems. When we look to the proposed topologies, we could say that the inputs are low impedance as the Δ Vin is almost zero thus implying that the impedance is near zero. While this might appear to be a problem, it is not. With a voltage amplifier, one attempts to generate as high an input impedance as possible so as not to affect the voltage input by drawing current. It is the case with this patent that we want to have as low an input impedance as possible so as not to affect the current input by generating a voltage difference at the input. This is also the case with the Inverting Input of a CFA. Many of the problems of the CFA revolve around the "non-zero impedance inverting input". A true zero input impedance would mean that even a small voltage input would produce infinity current into the input. This is not really needed or even desirable. As with a normal op amp, it is necessary that the loop resistors (components) are not "loaded" by the input current, i.e. that any current needed by the input do not "show up" on the feedback resistors. In other words, the input current should not affect the closed loop performance of the circuit. In the proposed circuit, it is desired that any voltage differences created by the amplifier's input impedances do not affect the closed loop performance of the circuit. We can see that in most of the embodiments, if one of the inputs is set at a certain voltage, the other input is to some degree locked to that voltage. Any input current will not change the voltage at the input of the circuit. In particular, if a current is fed into the circuit via an input resistor, then the whole driving voltage will be dropped across the input resistor. This is ideal. We see then that when dealing with voltages, that the closed loop input impedance of an configured embodiment/usage of the proposed circuit would just be that of the input resistor. This is nice as that is just what it is with a voltage-feedback amplifier. We see that a voltage imposed at the input end of the input resistance will cause to flow a current equal to V_{in} / R_{in}. In an open loop configuration using Figure 8, this will cause a voltage to drop across an output load (resistance) equal to $= -\beta^2 * R_L \bullet V_{in} / R_{in}$. Dividing each side by V_{in} gives us the open loop voltage gain as stated above $A_{ol} = -\beta^2 * R_L / R_{in}$. Using "current feedback" (sending back current into the summing point), to produce zero current at the summing point, means that $V_{out} / R_f = -V_{in} / R_{in}$. This becomes the same as with a voltage-feedback op amp, i.e. $V_{out} / V_{in} = -R_f / R_{in}$. The loop gain then becomes: Loop Gain $= (-\beta^2 * R_L / R_{in}) / (-R_f / R_{in}) = \beta^2 * R_L / R_f$.

An important difference then between the proposed amplifier topologies and that of a traditional CFA is that the proposed amplifier topologies have two balanced current inputs that draw small amounts of current to produce a desired results, whereas the traditional CFA has two unbalanced inputs only one of which is actually a current input but which demands a significant current. This decrease of current required is of the order of magnitude of from β to β^3, depending on the embodiment and whether it uses an output buffer or not. This decrease of input current is significant and makes the proposed circuit much easier to use and more able to get the performance desired than previous op amps including CFAs. We showed above that we can expect an input current of about 10nA as compared to 25 µA for prior art CFAs.

All the embodiments detailed here have good high frequency properties. One can further optimize the circuit for high frequency use by reducing the open loop gain and increasing the currents used internally. Examples of such are circuits in Figures 11and 12. Figure 11 is created from Figure 8 with the addition of transistors Q_{21}, Q_{22}, Q_{23}, and Q_{24} connected as diodes with bases connected to collectors. Figure 12 is created from Figure 10 with the addition of the same transistors as connected as diodes.

In these circuits the quiescent current of each of the transistors in the circuit is ½ I_{cc}. Therefore the frequency response of all areas of the circuit is much better than where the input stage is at a reduced level of current, even though the input stage is cascoded. The gain is reduced (by a factor of β). The transresistance of circuit 11 is $\beta * Z_L$ and circuit 12 is $\beta * Z_E$. These circuits give a clean roll-off and the ability to tailor the response for maximum bandwidth. With a better output stage than shown in figure 12, the results would be better yet. Expected results (with a Z_L of 1KΩ) for circuit 11 is a transresistance of 100KΩ with a break frequency of greater than 2500KHz for a product of 250×10^9. This is the same product as for the CLC401 as stated above but with a much simpler circuit, more options, easier to use and better specs in other areas. When we look to circuit 12, we see an improvement of an order of magnitude at least. The transresistance of circuit 12 with an internal resistance of 10K (R_E) is 1000KΩ with again a break frequency of greater than 2500 KHz for a product of 2500×10^9. This tells us that we can get a closed bandwidth of 500 MHz with a R_f of 5000. The circuit can be used either as an inverting or non-inverting gain amplifier. The closed loop frequency response is, as it is with CFAs in general, fairly independent of gain. Using an input resistor R_{in} of 500, we get a gain of 10 with the bandwidth of 500 MHz. Increasing R_E or replacing it with a capacitor or using high frequency transistors would increase these figures.

In Figure 13, we see one further set of ways to use the circuit. Using one output to drive a non-inverting input of the other output, we get a still further increase of transresistance. We see the transresistance is = $\beta^2 * R_L$ $[(Z_x + (\beta + 1) Z_y) / (Z_x + Z_y)]$. By making Z_x "small", we get an improvement of $(\beta + 1)$ in transresistance. The simplest case is just to delete Z_y and connect B to C in Figure 6. An added benefit would be that we would now have "lost" the non-inverting input altogether, which can be very useful indeed. We could also make Z_x and Z_y frequency dependent and thus tailor/enhance either the AC or DC performance of the amplifier. The common mode voltage for the circuit will be the reference voltage used by the output load and input.

A special note here is in order. With a voltage amplifier, one must be alert to shorts on the outputs. One can leave an output open or lightly loaded with a large resistor or a small capacitor. Anything more can disrupt the circuit.

With a current amplifier, the concern is opposite. One needs to be concerned with any open loads. An open load would cause the output to swing widely in both directions and possibly saturate at the supply rails. An unused output would best be loaded by a resistor or capacitor. This prevents it from saturating unpredictably. This is, of course, not the case with those circuit that use a voltage buffer on the output. These circuits are generally internally loaded and so can tolerate an open output. In fact, such buffers are not happy with a highly loaded or shorted output. Using the proposed topologies, the amplifiers which have an output voltage buffer still have the benefit of having current inputs.

All of the embodiments as detailed above and in the referenced Figures demonstrate examples of means as included in the Claims, in particular Claims 1, 2 and 3. All the embodiments except Figure 13 show two inputs that are responsive to currents. Figure 13 actually shows how to use the two inputs of Figure 6 to get a new special circuit as detailed in Claims 11 and 13. All the circuits have low enough offsets that feedback can be applied successfully. In fact some have very low offsets as detailed above. All the circuits show inputs that are substantially equal. Hard to see how one could make them more alike. Most of the embodiments show amplifiers which are totally symmetrical. All the amplifiers have at least one input that is an inverting input for one of the outputs. So all means elements of Claims 1, 2 and 3 are shown multiple times in the embodiments detailed in this application.

From the forgoing, it should be clear that the present invention may be embodied in forms other than those described above. The above-described examples are therefore to be considered in all respects illustrative and not restrictive or limiting, the scope of the invention being indicated by the appended claims rather than the foregoing. All changes that come within the meaning and scope of the claims are intended to be embraced therein